Chapter 20
Foundry Technologies Focused on Environmental and Ecological Applications

Ya. Roizin, M. Lisiansky, and E. Pikhay

Abstract Solutions allowing fabrication of remote control systems with integrated sensors (motes) were introduced as a part of CMOS foundry production platform and verified on silicon. The integrated features include sensors employing principles previously verified in the development of ultra-low power consuming non-volatile memories (C-Flash, MRAM) and components allowing low-power energy harvesting (low voltage rectifiers, high –voltage solar cells). The developed systems are discussed with emphasis on their environmental and security applications.

Keywords Sensor • RFID • Solar • NVM

20.1 Introduction

Information exchange and data processing systems, databases, etc., require modern VLSI operating at high frequencies and allowing low power consumption. The corresponding products follow the general scaling trend: "Moore's law" [1]. Semiconductor industry developing electronic systems for environmental, security and ecological security applications faces a new development concept: "More-than-Moore". In this case, designers less struggle for more advanced technology nodes, but intend to provide added values by incorporating new functionalities integrated in the CMOS platforms (both at the FE-front end and BE-back end levels of process flows). The functional diversification of "More than Moore" concept includes features delivered , e.g., by "mixed signal Analog/RF" and "HV/Power" technologies, includes 3-D structures, MEMS, embedded CMOS NVM and embedded memories

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of other types (e.g., MRAM.). Various sensor devices based on the mentioned technologies (e.g. MEMS accelerometers, specialized CMOS image sensors, sensors for measuring temperature, radiation, etc.) are integrated in the "More than Moore" systems. Corresponding semiconductor foundries are often considered "analog" foundries to distinguish them from "plain vanilla" CMOS foundries focused on production of microprocessors and other logic circuits and typically targeting advanced technology nodes (45–22 nm). "More than Moore" approaches became a part of Tower Semiconductor Ltd. (TSL) technology development strategy. This concept supposes a variety of applications, in particular connections with different fields of human activity, including control of environmental and ecological conditions, civilian and military intelligence. Actually, it gives an opportunity to step up from discrete sensors measuring speed, acceleration, pressure, flow, distance, field, temperature, humidity, concentration of contaminants, etc. by electronic means to sensor systems with increasing functionality: analog, digital, or mixed signal. Early digitalization and digital signal processing allow maximum use of integration benefits: application-specific algorithms, enabling error correction, faster signal processing, higher resolution, and lower energy consumption. A sensor system integrated on the CMOS design platform (system-on-chip, SOC) together with other features, like embedded NVM (non-volatile memory), RF CMOS, epitaxial SiGe enabling ultrahigh frequencies, etc. and supplied with energy harvesting elements (integrated solar batteries, on chip antennas) turns this sensor system into a small sized device that can operate autonomously in remote regime and sense environmental conditions, gather civilian and military information.

Robust integration of novel approaches into the existing CMOS platform is complicated. It is requested that the integrated features would not deteriorate the basic CMOS process or make the total process flow too complex. In particular it is requested that: (i) changes of the core CMOS devices fabricated on the same wafer would be minimized; (ii) the introduced new functionality would not lead to unreasonable increase of the chip area. Strict low cost policy is applied for most applications (typically, only 1–2 additional masks to the core CMOS process).

The present paper describes diverse embedded features introduced into TSL production technologies. These features (some of them employing nanoelectronic principles) enable fabricating of chips for environmental ecological and security systems within conventional CMOS processes (0.13 and 0.18 μm technology nodes).

20.2 Devices Integrated into the Core CMOS Platform

20.2.1 RFID Platform Demonstrator

By Motes and/or Smart Dust we have in mind small-sized semiconductor devices that can sense environmental conditions and gather civilian and military intelligence. Motes can, in principle, communicate with each other and transmit data to a

Fig. 20.1 RFID demonstrator
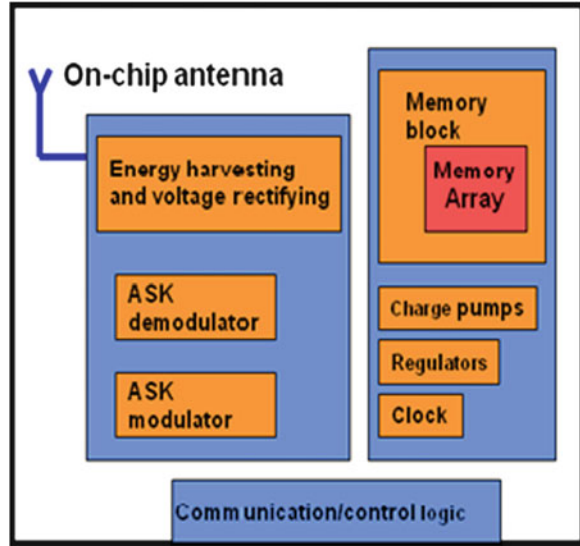
command center. This way information, e.g. about disasters, contaminations, or tags distributed to stick to suspects or their vehicles could be gathered and preliminary processed. Smart Dust are, actually, tiny microcomputers connected into a wireless net that record and transmit information [2]. TSL RFID demonstrator is a low-power chip having attributes of a standard RFID system but specially designed to allow integrating of diverse sensor features. In this paper we will focus on several original integrated sensor technologies and special non-volatile memories that enable the requested demonstrator functionality and ultra-low power operation. Figure 20.1 shows the block diagram of the RFID demonstrator. The demonstrator consists of three functional units: memory module, RF module (including on-chip antenna) and digital controller. The RF module performs two functions: first, it establishes the radio communication of the chip with the external reader device, and second, it harvests the electromagnetic energy to provide the DC power for the chip. A distinguishing feature is utilizing TSL Schottky CoSi diodes with low V_{ON}. CoSi diodes allow to rectify very small voltages generated by the on-chip antenna (compared with standard rectifiers built on p-n diodes that work at V > 0.5 V). A cross-section of a CoSi diode implemented in RFID designs is shown in Fig. 20.2 [3].

The memory block is based on the ultra-low power C-Flash memory cell, described in the Sect. 20.2.2. The digital controller manages the chip supporting the basic communication protocol.

20.2.2 Ultra-Low Power Consuming NVM

C-flash memory is a single poly EEPROM integrated into CMOS 0.18 μm node technology [4, 5]. Figure 20.3a, b shows the schematic and 3D view of the memory cell.
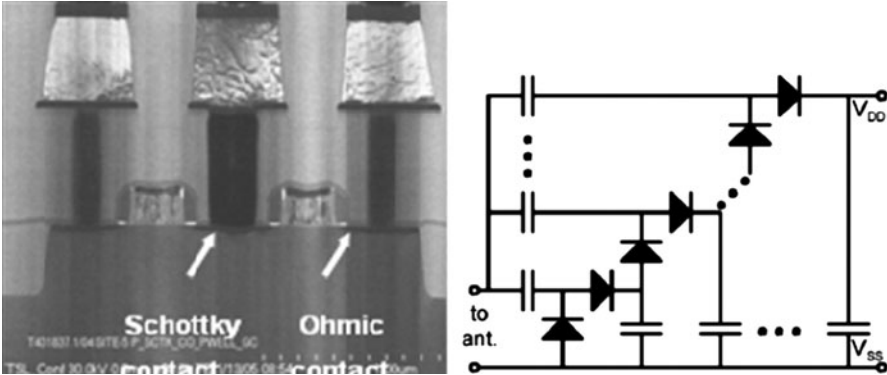
Fig. 20.2 Zero cost CoSi Schottky diode and schematic illustration of its application. Features: zero cost; high Ft (>90 GHz); low capacitance (~3.0 fF/μm^2); in the read mode RF harvester allows $V_{DD} > 1.2$ V, I $\approx$ 10 μA
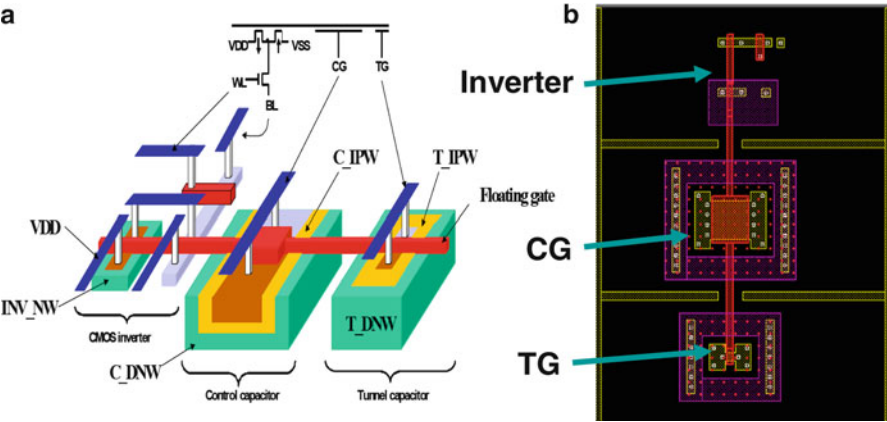

Fig. 20.3 C-Flash memory: (**a**) schematic and 3D view; (**b**) layout of C-Flash memory cell

Actually, C-Flash memory cell consists of a CMOS inverter with a common Poly Floating Gate (FG) that is coupled to two capacitors: the large and the small area ones, that are called control gate (CG) and tunneling gate (TG), respectively (70 Å thermal SiO_2 serves as the gate oxide). Each of capacitors is isolated by placing into an individual P-well (IPW). Programming/erasing of the cell is performed by applying the voltage between the capacitors: the most part of the applied voltage drops on TG. The typical operation regimes of the cell are presented in Table 20.1.

Fowler-Nordheim (F-N) tunneling mechanism of programming together with negligible current of inverter in readout regime ensure ultra-low power consumption of the memory cell. This feature is a crucial requirement for considering the C-Flash memory as a candidate for RFID applications. Two-polarity operation allowing the use of voltages at the level supported by CMOS 0.18 μm node

Table 20.1 C-Flash operation regimes

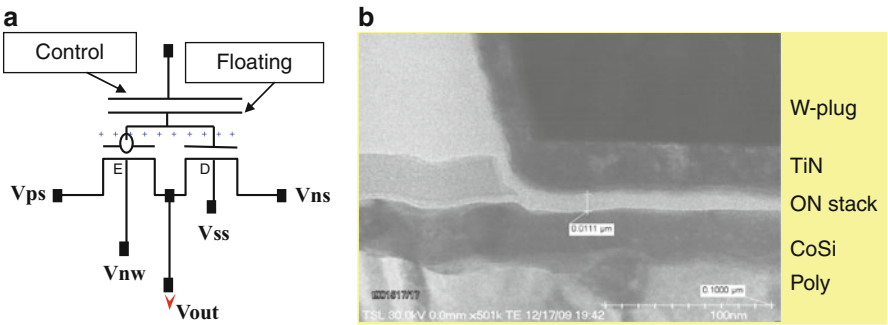| Terminal	Program	Erase	Read
VDD	0	0	1.8 V
VSS	0	0	0
VCG	4.75 V	−4.75 V	SWEEP
VTG	−4.75 V	4.75 V	0
VC_DNW	4.8 V	0	MAX_SWEEP
VT_DNW	0	4.8 V	0
INV_NW	0	0	1.8 V
WL	0	0	3 V
BL	–	–	Sensing

Fig. 20.4 (**a**) Schematic view of C-Flash memory cell (1-cap modification); (**b**) SEM image of W-plug cross-section

technology is an additional benefit. The cell shown in Fig. 20.3b has a relatively large area ~35 μm^2 (though much smaller compared with competing solutions) [6].

The area can be reduced using an original 3D gate structure [7]. Control gate metal electrode (W-plug) alters the ideology of the cell design, making it closer to the design of "classical" EEPROM [7, 8]. A schematic view of the readout part of the C-Flash memory cell is shown in Fig. 20.4a. In this case, W-plug electrode with inter-gate dielectric (see Fig. 20.4b) plays the role of the CG capacitor.

The CG capacitor is located on STI which ensures additional advantages of W-plug C-Flash memory cell over other NVM solutions:

(i)   Low parasitic capacitance to ground (minimization of AC power consumption)
(ii) Smaller cell area (W-plug CG capacitor is placed in the area that separates NMOS and PMOS transistors of the CMOS inverter; according to the design rules, the minimum distance is ~1.5 μm).

Besides the mentioned advantages, the metal electrode concept makes feasible an advanced option: a 3D trench CG capacitor that allows further reducing of the cell area to ~5 μm^2 (instead of 10–12 μm^2 demonstrated on silicon) [9]. The W-plug

**Fig. 20.5** SEM cross-section of MTJ magnetic cell
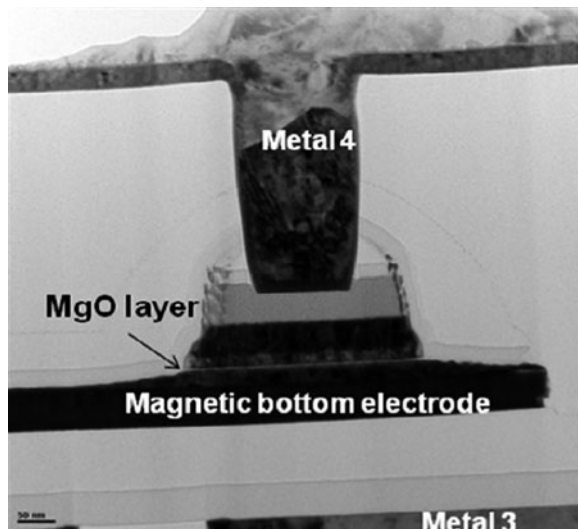
CG capacitor has excellent dielectric properties ensuring excellent endurance (1 M cycles) and perfect retention parameters.

20.2.3   Magnetic Elements

Figure 20.5 shows the TA (thermally assisted) MTJ (magnetic tunnel junction) element developed by TSL together with Crocus Technologies and integrated into the BE of TSL 0.13 µm process flow [10].

The cell includes a reference layer with fixed magnetic polarization and a storage layer with free polarization separated by a tunnel (MgO) dielectric. The sensor is read out by forcing a small current through the MTJ. This current is higher if both storage and reference layers are polarized in the same direction. After heating the MTJ by a short pulse of current, the system becomes sensitive to external magnetic field. The sensor is "programmed" using a specially dedicated "field" line that creates magnetic field in the vicinity of MTJ. After forcing heating current and exposing to the external magnetic field with the "field" line off, one can register external magnetic fields (several sensors with different orientation of magnetic polarization are tested in parallel). The sensitivity of the described sensor is of the order of tens of Öe. MTJ employs MgO layer with a thickness of ~15 Å. The dot diameter is ~200 nm. The advantage of the described solution is a very small measurement time (of the order of 10 ns) and high sensitivity. It is clear that the proposed principle can be employed in MRAM nonvolatile memory .Such memory is currently developed together with Crocus Technology and can be implemented in future systems for ecological control.

Fig. 20.6 Layout and schematic diagram of integrated radiation sensor
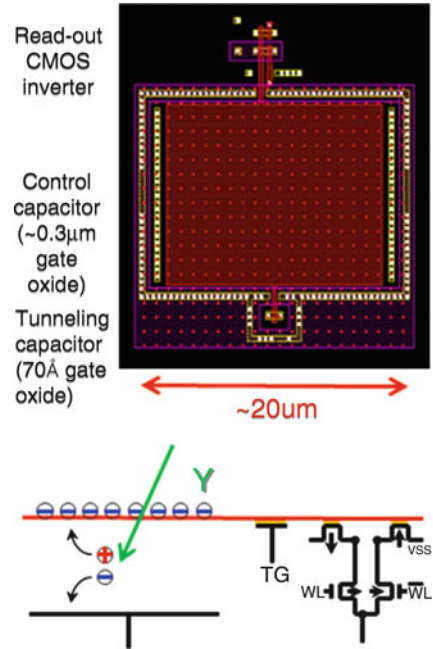
20.2.4 *Integrated Radiation Sensor*

To create a radiation sensor integrated into the RFID system, modification of the described above ultra-low power C-Flash NVM cell is performed to make the device more sensitive to radiation. This is achieved by replacing thin (70 Å) gate dielectric by thick STI isolation oxide (3,500 Å) under the floating gate of C-Flash cell in the control capacitor region, as shown in Fig. 20.6. γ-photons absorbed in the thick STI produce e-h pairs that reach the precharged floating gate and discharge it. The amount of charge in the floating gate can be determined from the electrical measurements (channel current in one of C-Flash complementary pair transistors, or CMOS inverter output voltage). The total absorbed dose (TID) can be easily calculated from the collected data. Two sets of C-Flash radiation sensors were prepared for irradiation. The floating gates of corresponding sensors were charged positively and negatively. Then, the cells were divided into several groups. The cells from each group were exposed to different doses of Co^{60} radiation that corresponded to 1, 2, 5, 10 and 20 krad absorbed doses (Si). The V_t values of cells before and after the irradiation are presented in Fig. 20.7. Clear correlation between the absorbed dose and the final V_t is observed. The dose of 1 krad resulted in pronounced V_t shifts, and the dose of 20 krad discharged the cells completely.
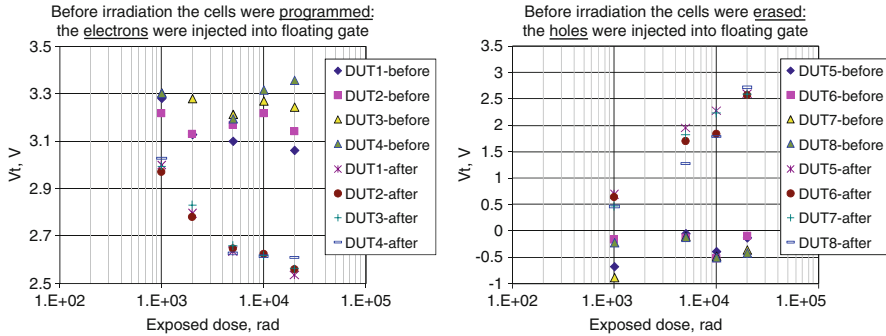
Fig. 20.7 Demonstrating the dosimeter function of modified C-Flash cell

20.2.5 Embedded High Voltage Solar Cells

Besides the sensor elements, RFID demonstrator is supplied with an original back-up solar voltage source. The distinguishing feature of the integrated solar battery is high generated voltage (10–15 V and above). The design of the battery and its layout is illustrated in Fig. 20.8a. The battery consists of a series of vertical p-n junctions connected by salicide metal stripes. A typical loading characteristic for such a battery implemented on SOI and used for driving of an embedded MEMS sensor is shown in Fig. 20.8b. Though the currents are relatively low (small photosensitive area), the developed power is enough to drive certain types of embedded devices and serve as a back-up to RF harvesting module.

20.3 Conclusions

We have demonstrated several "More than Moore" embedded features in TSL 0.18 and 0.13 μm production platforms. Ultra-low power single Poly embedded NVM and radiation sensors based on the floating gate principle, sensors employing magnetic tunnel junctions and high voltage solar batteries were designed and verified on silicon. Corresponding devices were developed as a part of the work on TSL RFID demonstrator which allowed fabricating remote motes with the ability to record parameters important in environmental and ecological monitoring.
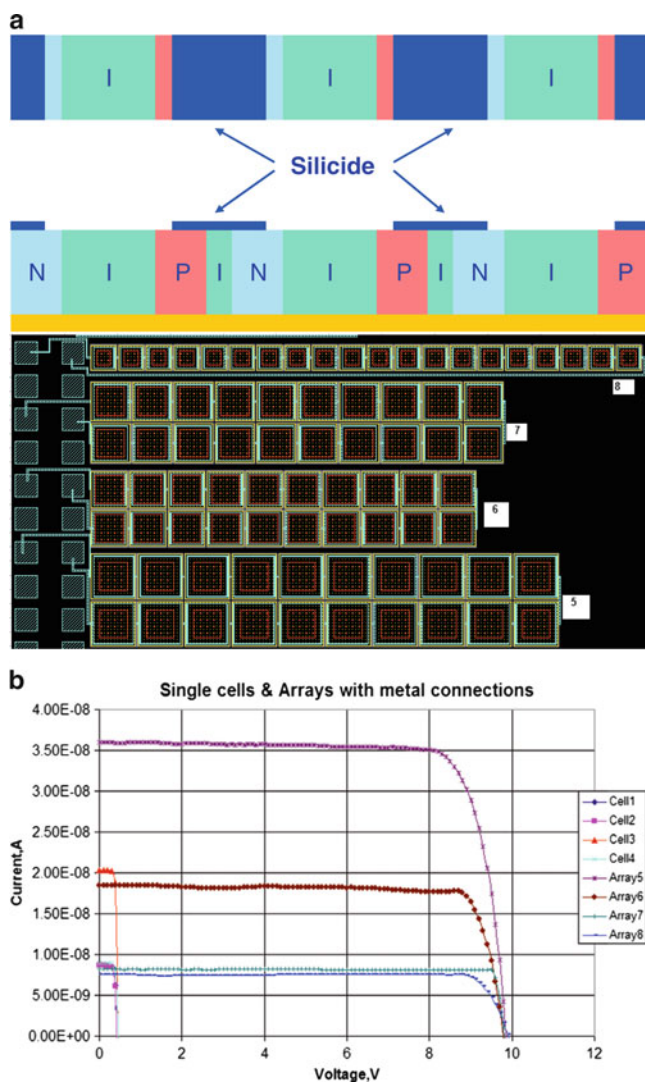
Fig. 20.8 (**a**) Solar battery principle and layout; (**b**) solar battery loading curves (low illumination)

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