Chapter 21
Electronic Noise in Deeply Scaled Nanodevices

C. Pace

Abstract Low frequency noise represents one of the most powerful tools to investigate the defect density and the conduction mechanisms in deeply scaled nanodevices such as MOSFETs. As the size of new generation devices shrinks towards the nanometric scale, the noise level can influence the correct operation of the circuits. In this paper, we illustrate the basic information needed to perform noise measurements, some references to the instrumentation involved and a few examples on how the noise investigation can be of help in the evaluation of the quality of innovative MOSFET gate stacks where high-*k* materials are implemented as gate dielectrics.

Keywords Electronic noise • Low-noise instrumentation • MOSFET • High-k

21.1 Introduction

Electronic Noise, at first sight, can be considered a problem. It can be identified as the random fluctuation of voltages and currents, which is present in every electronic device and hence circuit. It is an effect of physical phenomena occurring at microscopic level, such as interaction of charge carriers with host lattice or defects. But it can also turn in a chance if is used as a way to have an insight into charge transport mechanisms or a diagnostic tool for the device quality and reliability.

C. Pace (✉)
Department of Electronics, Computer Science and Systems,
University of Calabria, Via P. Bucci 42C, 87036 Rende, Italy
e-mail: cpace@unical.it

Y.N. Shunin and A.E. Kiv (eds.), *Nanodevices and Nanomaterials for Ecological Security*, NATO Science for Peace and Security Series B: Physics and Biophysics, DOI 10.1007/978-94-007-4119-5_21,

21.2 Noise Theory

21.2.1 Time-Domain Parameters

If we deal with the time evolution of a physical quantity, we can define a process as stationary if averages are independent of time (Fig. 21.1).

The simpler average that can be taken in to account is the mean value, defined as

$$\bar{x} = \lim_{\tau \to \infty} \frac{1}{T} \int_{-\frac{\tau}{2}}^{+\frac{\tau}{2}} x(t)dt.$$

Usually, noise is defined as the variation around the mean value, thus the noise mean value is assumed to be zero. In this case the mean square value can be defined as

$$\bar{x}^2 = \lim_{\tau \to \infty} \frac{1}{T} \int_{-\frac{\tau}{2}}^{+\frac{\tau}{2}} x^2(t)dt.$$

The last quantity, if referred to a voltage or current signal, can be interpreted as the average available power normalized with respect to 1 Ω load resistor.

The most important time domain statistical parameter is the root mean square value, defined as

$$x_{rms} = \sqrt{\bar{x}^2} = \sqrt{\lim_{\tau \to \infty} \frac{1}{T} \int_{-\frac{\tau}{2}}^{+\frac{\tau}{2}} x^2(t)dt}$$

and expressed in Volt or Ampère for voltage or current signals, respectively.

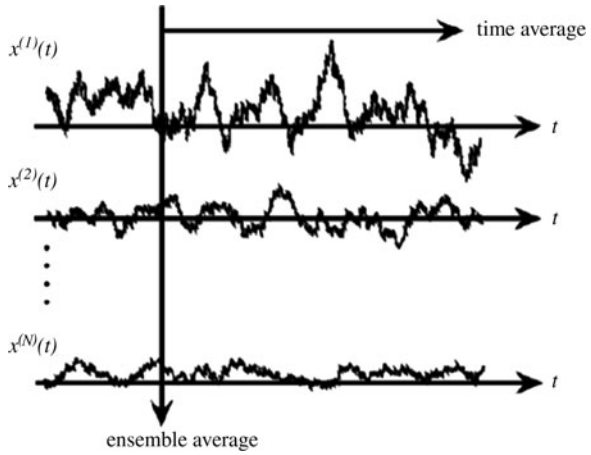

Fig. 21.1 Time-domain plot of an ensemble of N signals

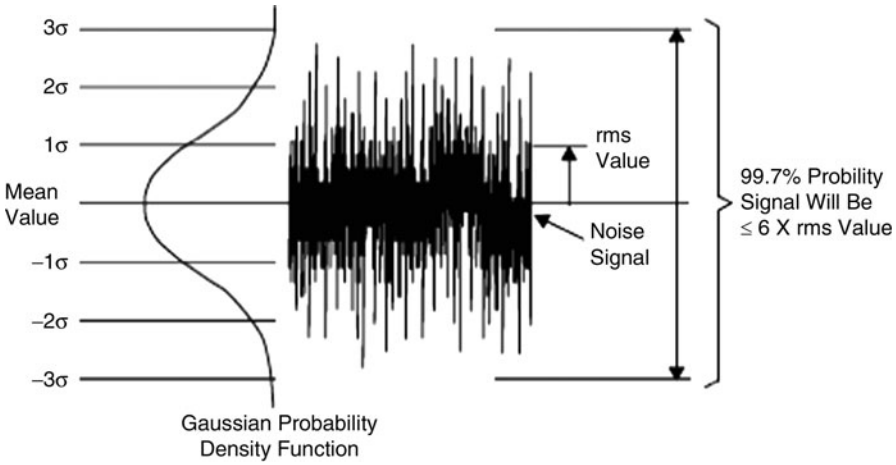

Fig. 21.2 Example of Gaussian amplitude distribution of a noise signal

The noise performances of electronic devices, such as operational amplifiers, are often declared in this form by the manufacturer.

Noise sources often present a gaussian amplitude distribution defined, for zero mean value signals, by the formula

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{x^2}{2\sigma^2}}.$$

21.2.2 Frequency-Domain Parameters

Using the Fourier transform, a random signal can be evaluated in the frequency domain, expressing it in terms of Power Spectral Density (PSD).

$$S_x(f) = \int_{-\infty}^{\infty} x(t) e^{-j2\pi ft} dt.$$

This is the most important frequency domain statistical parameter. It allows the calculation of the noise power comprised between the frequencies f_1 and f_2

$$P_x(f_1 \leq f \leq f_2) = \int_{f_1}^{f_2} S_x(f) df.$$

It is expressed in V^2/Hz or A^2/Hz for voltage or current signals, respectively. It is also common to take the square root of $S_x(f)$, expressing the result in V/$\sqrt{}$Hz or A/$\sqrt{}$Hz.

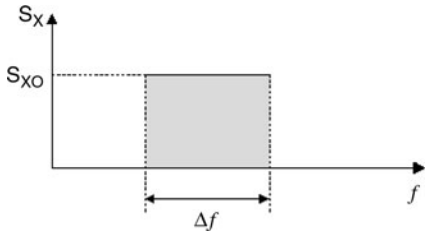

Fig. 21.3 Example of calculation of time-domain quantities from the PSD of a noise signal

The relationships between time-domain and frequency domain quantities are expressed by the following formulae

$$\overline{x^2} = \int_0^\infty S_x(f)df$$

$$X_{rms} = \sqrt{\int_0^\infty S_x(f)df}$$

A simple example can be the calculation of the time-domain quantities for a noise characterized by a constant PSD, as illustrated in Fig. 21.3, where:

$$\overline{x^2} = S_{X0}\Delta f; \quad X_{rms} = \sqrt{S_{X0}\Delta f}$$

Nevertheless, measuring systems produce sample records, not mathematical functions, so the PSD can not be analytically calculated. In practical cases, to evaluate the spectral properties of a signal, we can make use of the Discrete Fourier Transform (DFT):

$$X[k] = \sum_{n=0}^{N-1} x[n]e^{-j\frac{2\pi kn}{N}} \quad k = 0, 1, ..., N-1$$

A signal record of N samples becomes a set of $N/2$ DFT values, as in Fig. 21.4.

So, using the DFT, the PSD of a signal can be evaluated from the sampled data in the following way, obtaining the so called one-sided spectrum.

$$S_x(k) = 2\frac{|X_{DFT}(k)|^2}{f_S N}.$$

The PSD will be evaluated in a discrete number of frequencies, starting from a minimum value f_{min}, also equal to the frequency step Δf, whose value is

$$f_{\min} = \Delta f = \frac{1}{NT_S}$$

and ending to a value f_{max} determined by the sampling frequency f_S as

$$f_{\max} = \frac{f_S}{2},$$

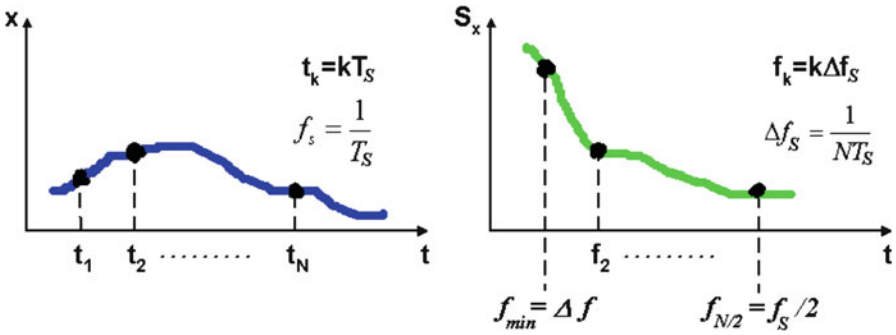

Fig. 21.4 Calculation example of DFT coefficients from the signal sample record

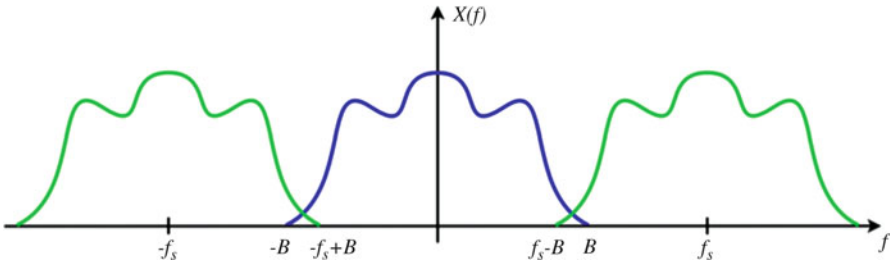

Fig. 21.5 Aliasing problem: *blue curve* is the PSD of the original signal, *green curves* are the first replicas of the reconstructed signal after a wrong choice of the sampling frequency

where T_S is the sampling interval and N is the total number of samples acquired in the time record of length $T = NT_S$.

Some considerations apply to the DFT estimation of the signal PSD:

1. the minimum estimated frequency equal the inverse of the total acquisition time T. So investigations in the low-frequency region of the spectrum will take a long time during which the stationarity of the process have to be guaranteed in order to obtain meaningful results;
2. the maximum estimated frequency equals half the sampling frequency f_S. So to investigate the characteristics of the signal in the high frequency region, we need to acquire faster and manage a significant amount of data per second.

In order to correctly evaluate the signal PSD it is necessary to sample it according to the Nyquist-Shannon theorem, which provides that, for an exact reconstruction of a continuous-time signal from its samples, the signal must be band-limited and the sampling frequency must be greater than twice the signal bandwidth. Otherwise, the aliasing problem occurs, that is replicas of the baseband shape of the original signal will overlap in the reconstructed signal and hence spectrum (Fig. 21.5).

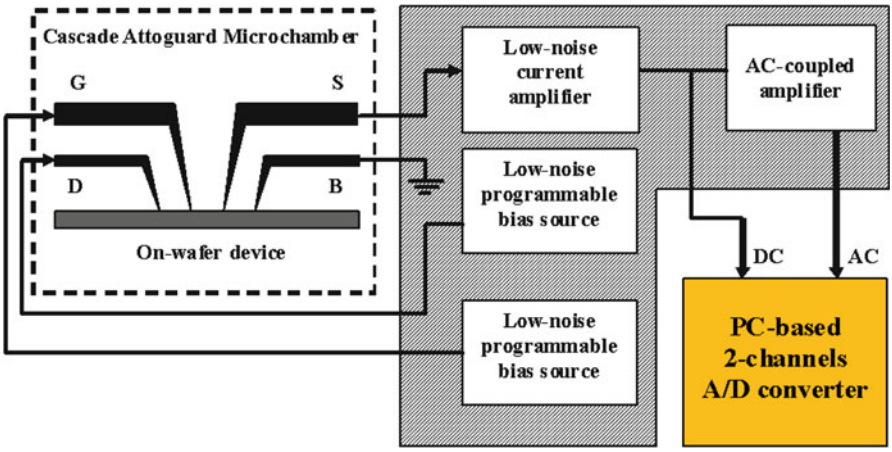

Fig. 21.6 Example of wafer-level low-noise acquisition system. The *gray shape* identify the ultra-low-noise programmable biasing and amplifying instrumentation

In order to guarantee that no significant power is present in the signal spectrum above the higher frequency considered, suitable devices such as Dynamic Signal Acquisition equipments have to be used to perform sampling. Such Analog-to-Digital converters are equipped with programmable anti-aliasing filters that adjust the cutoff frequency in relation to the sampling frequency selected. The NI 4462 DAQboard from National Instruments is an example.

21.2.3 Noise Measurement Techniques

The practical execution of noise measurements on deeply scaled nanodevices is not a trivial activity. The weakness of the voltage and current signals involved and the sensitivity to electrostatic damage of the devices that are almost always available at a wafer level, force the operator to work with great caution in order to obtain correct results. A possibility to speed-up the measurement procedure is to integrate into a single instrument the ability to perform the wafer-level static and noise measurements, without disconnecting the device between the ones and the others. An example is shown in Fig. 21.6 [1].

The user can program the instrument in order to perform the DC characterization of the Device Under Test (DUT) as in Fig. 21.7. Then the bias points of interest can be selected and an automatic sequence of noise measurements, as in Fig. 21.8, can be performed. These two main tasks are brought out by a digital section that controls the analog section and is interfaced to the PC through an optical interface. The digital section is almost completely shut down during noise measurement, setting its microcontroller (μC) in sleep mode.

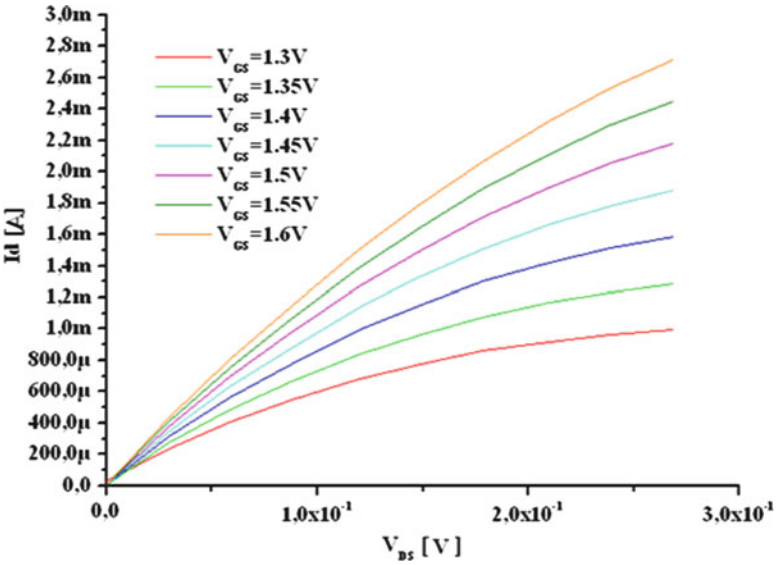

Fig. 21.7 Static characterization of a MOSFET for the identification of the noise measurement bias points

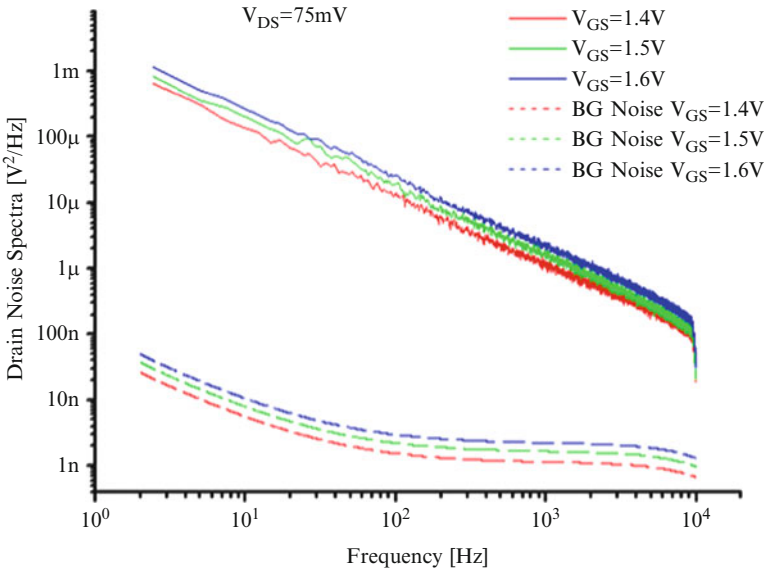

Fig. 21.8 Noise characterization of a MOSFET at different bias points. *Dashed curves* are the background noise estimation of the biasing-amplifying chain

Since the current of the MOSFET could be very low, especially for submicron devices, it's an imperative to adopt a very low noise biasing and amplification chain design in order to avoid that the background instrumentation noise would mask the device noise.

21.3 Study Cases: Defects Analysis of Advanced CMOS Gate Stacks

The restless push for more and faster devices on a chip in CMOS technology is driving the demand for shrinking geometries. The accompanying gate dielectric thickness decrease leads to a large gate-current leakage due to quantum mechanical tunneling of carriers through the thin gate oxide [2, 3] and, therefore, to higher static power dissipation.

That problem is alleviated in novel gate stacks by introducing high-*k* materials in order to achieve the same gate dielectric capacitance of conventional SiO2 with a thicker dielectric layer. It should be noted that, for decades, the quality of the silicon/silicon dioxide interface was a key feature of the silicon technology and a lot of effort has been put in order to replace the silicon dioxide with high-*k* dielectrics. Difficulties arise in order to address typical issues like threshold voltage shift, mobility reduction, bias temperature instability and stress-induced leakage current, which are common in high-*k* materials [4, 5].

On the other hand, several studies have shown that low-frequency drain-current noise measurements represent one of the most powerful tools to investigate the material defectiveness [6–11]; therefore, noise analysis is very useful to validate the quality of the gate stack when new materials are introduced. Furthermore, a new model has been recently proposed in [12], where it is shown that low-frequency gate-current $1/f$ noise can also be used as a source of information for assessing the quality of the gate stack in MOS structures.

This investigation technique is very suitable in the case of large gate-current leakage, where the accuracy of most traditional techniques (combination of high-frequency and quasi-static *C*–*V* [13], charge pumping [14, 15], and drain noise measurements) could be corrupted.

The idea behind this model [12] is that the charging/discharging of defects in the dielectric can block/unblock effective portions of the gate area, thus causing a fluctuation in the gate current. With this in mind, the gate noise is proportional to the total amount of traps that can be charged/discharged in the dielectric.

In the following will be shown how drain- and gate-current noise measurements have been used to check the quality of high-*k* gate stacks in MOSFETs.

The following Figs. 21.9, 21.10, 21.11, and 21.12 illustrate some experimental evidences that has been utilized [16] to localize the sources of gate-stack quality degradation in relation to the variation of several parameters: high-*k* material, interfacial layer (IL) thickness, strain engineering and substrate material.

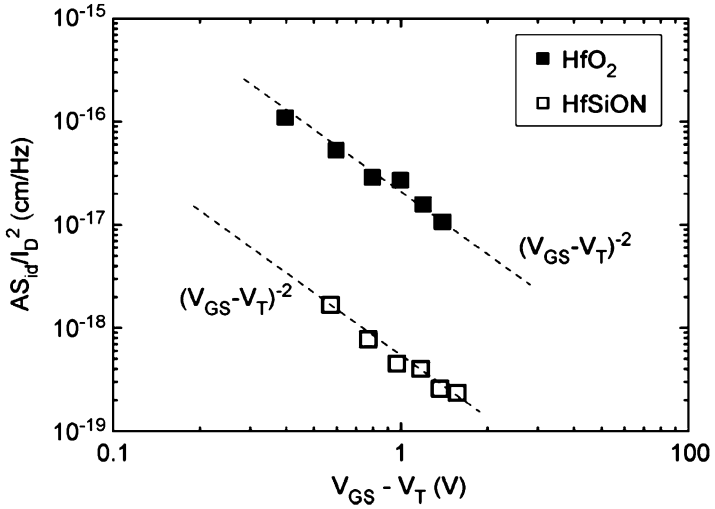

Fig. 21.9 Normalized drain-current spectral density at $f = 25$ Hz as a function of the gate voltage overdrive for different high-k dielectrics. In the measured devices, the channel width was 10 μm, while the channel length ranged from 0.18 to 0.25 μm. N-MOSFETs with HfO2 dielectric show one decade higher noise than the ones with HfSiON

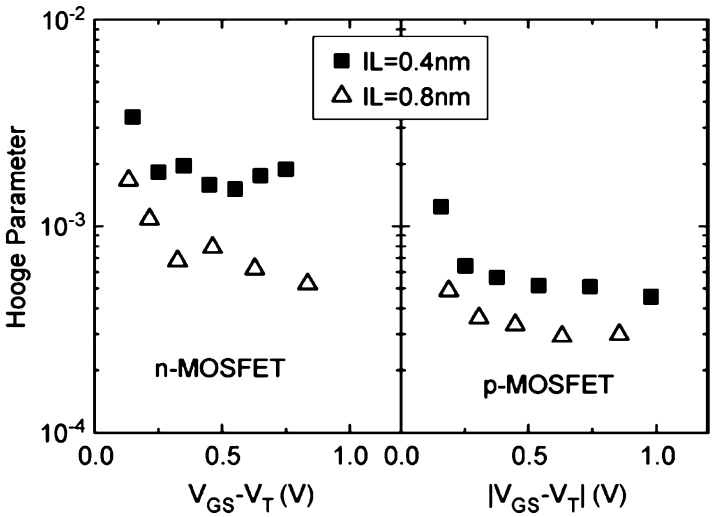

Fig. 21.10 Hooge parameter values extracted for n-MOSFETs and p-MOSFETs with different interface layer (*IL*) thicknesses. The MOSFETs had $W = 10$ μm and $L = 1$ μm. In both types of MOSFETs, the Hooge parameter increases when the IL decreases

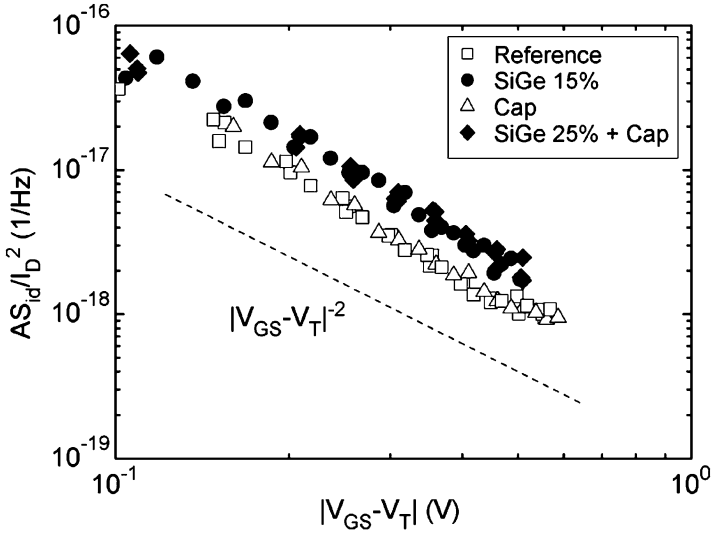

Fig. 21.11 Normalized drain-current spectral density at $f = 25$ Hz as a function of the gate voltage overdrive for p-MOSFETs with different strain engineering: unstressed reference, 15% SiGe S/D, Si3N4 cap layer, and 25% SiGe S/D + Si3N4 cap layer. In all the cases, the investigated devices were 10 μm wide and 1 μm long

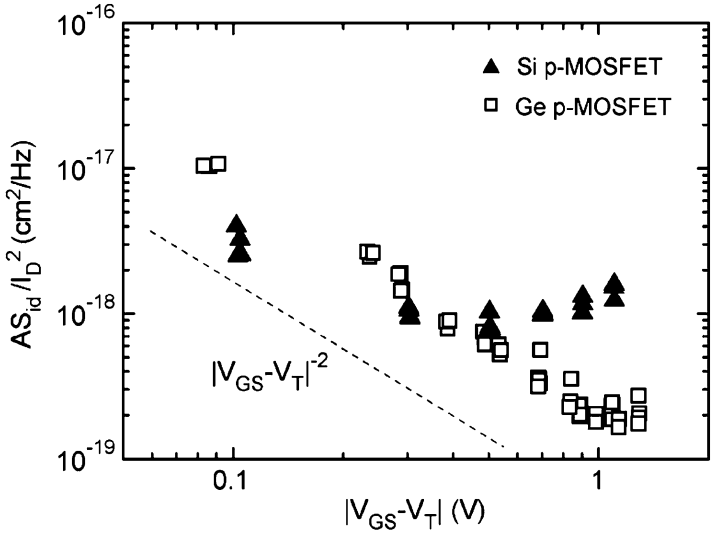

Fig. 21.12 Normalized drain-current spectral density at $f = 25$ Hz as a function of gate voltage overdrive for p-MOSFETs with different substrates: Silicon or germanium. For both devices, we investigated channel widths of 10 μm and channel lengths of 1 μm. The noise seems to be slightly higher for Ge p-MOSFETs at low gate voltage overdrive

References

1. Pace C, Piacente A, Vescio F, Pierro S, Dalia R, Singh Bisht G (2010) An ultra-low-noise source-measuring unit for semiconductor device noise characterization. In: Proceedings of IEEE-I2MTC 2010, Austin, TX, pp 3–6
2. Semiconductor Industry Association (2007) International technology roadmap for semiconductors, San Jose, CA. http://www.itrs.net/reports.html
3. Houssa M, Pantisano L, Ragnarsson L-Å, Degraeve R, Schram T, Pourtois G, De Gendt S, Groeseneken G, Heyns MM (2006) Electrical properties of high-κ gate dielectrics: challenges, current issues, and possible solutions. Mater Sci Eng 51(4–6):37–85
4. Wilk GD, Wallace RM, Anthony JM (2001) High-κ gate dielectrics: current status and materials properties considerations. J Appl Phys 89(10):5243–5275
5. Baklanov M, Maex K, Green M (2007) Dielectric films for advanced microelectronics. Wiley, New York
6. Hooge FN (1994) *1/f* noise sources. IEEE Trans Electron Device 41(11):1926–1935
7. Hung KK, Ko PK, Hu C, Cheng YC (1990) A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors. IEEE Trans Electron Device 37(3):654–665
8. Simoen E, Mercha A, Pantisano L, Claeys C, Young E (2004) Lowfrequency noise behavior of SiO2 − HfO2 dual-layer gate dielectric nMOSFETs with different interfacial thickness. IEEE Trans Electron Device 51(5):780–784
9. Ghibaudo G, Roux O, Nguyen-Duc C, Balestra F, Brini J (1991) Improved analysis of low frequency noise in field-effect MOS transistors. Phys Status Sol A 124(2):571–581
10. Kirton MJ, Uren MJ (1989) Noise in solid-state microstructures: a new perspective on individual defects, interface states, and low-frequency noise. Adv Phys 38(4):367–468
11. Giusi G, Crupi F, Pace C, Ciofi C, Groeseneken G (2006) A comparative study of drain and gate low frequency noise in nMOSFETs with hafnium based gate dielectrics. IEEE Trans Electron Device 53(4):823–828
12. Magnone P, Crupi C, Iannaccone G, Giusi G, Pace C, Simoen E, Claeys C (2008) A model for MOS gate stack quality evaluation based on the gate current *1/f* noise. In: 9th international conference on ultimate integration of silicon, Udine, Italy, pp 141–144
13. Schroder DK (2006) Semiconductor material and device characterization. Wiley, New York
14. Groeseneken G, Maes HE, Beltràn N, De Keersmaecker RF (1984) A reliable approach to charge-pumping measurements in MOS transistors. IEEE Trans Electron Device ED-31 (1):42–53
15. Zahid MB, Degraeve R, Zhang JF, Groeseneken G (2007) Impact of Process Conditions on Interface and High-k Trap. Density Investigated by Variable $T_{CHARGE} - T_{DISCHARGE}$ charge pumping (VT2CP). Microelectronic Eng 84:1951–1955
16. Magnone P, Crupi F, Giusi G, Pace C, Simoen E, Claeys C, Pantisano L, Maji D, Ramgopal Rao V, Srinivasan P (2009) 1/*f* noise in drain and gate current of MOSFETs with high-*k* gate stacks. IEEE Trans Device Mater Reliab 9(2):180–189