Chapter 31
Nanoparticles in Gate Dielectric of Memory Transistors

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Abstract A computer model of nanoparticles in the gate dielectric of memory transistors is studied. We propose a special approximation for dielectric constant at small distances for description of dielectric properties of nanoparticles. The temperature dependence of the dielectric constant, ε (T) is accounted. It has been found that a difference between ε (T) inside and outside the nanoparticles significantly determines their trapping properties.

Keywords Nanoparticles • Dielectric constant • Memory transistors

31.1 Introduction

31.1.1 Single Electron Devices

Within the last decade single electron devices (SED) with discrete nanocrystal charge-storage sites have been fabricated and widely used. In these devices charge-storage sites are nanoclusters embedded into a dielectric layer (for example Si_3N_4 in ONO devices [1]). SED allow controlling the number of electrons in the trapping centres one by one.

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A metal – or semiconductor – based SED should accumulate some number of electrons which have to provide the device operation. According to the definition: "SED should use addition or subtraction of one electron to/from an electrode to realize a digital bit". Another definition is: "SED utilizes for its operation one-electron-precision charge transfer based on the Coulomb blockade effect ". In the last case the number of electrons transferred between electrodes might be 100–1,000, but within one-electron precision. However, a better control of the electron count dictates to use a smaller number of electrons in the operation [2].

Nanocrystal memories (NCM) are based on the trapping of few electrons by nanoparticles. The charge is not stored in a continuous floating gate, as in the case of ONO, but in a discontinuous layer composed by numerous discrete traps-nanoparticles (TN) well separated one from the other [3]. The advantage of these devices is the ability to achieve faster programming speeds and the longest retention.

The nanocrystal layer has to meet certain specifications in order to support properly functioning memory devices. The first requirement is a given density of TN. The second is the thickness of the dielectric layer separating TN and the substrate that should be well controlled. Poor control of the tunnel oxide thickness results in wider threshold voltage distributions and increases the number of erratic bits [3]. The devices based on the Coulomb blockade effect must operate at room temperature, and these devices require TN of nanometre size (~2–5 nm) [4]. Typically, a regular size of Si TN is ~8 nm [5, 6].

The following advantages can be indicated for the new NCM in comparison with ONO memories:

1. Good scalability is linked to the operating principle based on the Coulomb repulsion of electrons. NCM device is anticipated to operate with very small physical dimensions, making possible an ultra-large scale integration.
2. In NCM the ordering of the trapping sites is controllable, while in ONO memory the ordering of the trapping sites is based on the random distribution of the dangling bonds and other defects, therefore the randomness of the trap sites causes a severe dispersion in the threshold voltage.
3. Ultra-low power operation of NCM is the result of a small number of electrons to accomplish the basic operation.
4. The extremely high speed of operation is an important feature of NCM. In conventional devices about 10^5, electrons are charged/discharged for a basic digital operation. In SED only a few electrons are transferred, therefore, the operation processes might be much faster.
5. The trapping probability is larger for NCM devices in comparison with ONO devices. It is caused by a large size of TN. These sizes of TN lead to significantly large cross-sections in trapping kinetics.

Using TN as memory reservoirs in memory transistors, it is possible to fabricate devices with unique properties. To model parameters of these devices we should describe physical characteristics of the gate dielectric, in particular, a dielectric constant in nanoscale distances. In this paper we demonstrate the approach that allows solving this problem.

31.1.2 Microscopic Model of Dielectric Constant

Dielectric constant is a macroscopic characteristic and has a sense at distances much larger than interatomic distance a_0. However, in the modelling of electronic processes in nanoparticles embedded into gate dielectric of memory transistor we should consider interactions at distances from $x \approx a_0$ to $x \approx a_0$. With this aim we suggest an approximation to describe ε simultaneously at small and large distances. For $x \approx a_0$ the dielectric constant corresponds to vacuum value, ε_V and for $x \approx a_0$ we use the value of bulk, ε_B. Thus, for the interval $x \approx 10–15a_0$ we have:

$$\varepsilon = \varepsilon_V + \beta x, \tag{31.1}$$

where 10 β $a_0 \approx \varepsilon_B$.

Different effects determine the temperature dependence of a dielectric constant [7]. One of them is the decrease in the number of polarisable molecules per unit volume as the temperature increases. For this case the dielectric constant can be written as:

$$\varepsilon = \varepsilon_0 + \alpha T, \tag{31.2}$$

where ε_0 is a dielectric constant at room temperature, T is the temperature. The coefficient α depends on the electronic properties of the substance and appears significantly different inside and outside the nanoparticle. Injected electrons have an accelerated temperature and as a result of electron-phonon interactions the lattice temperature in vicinity of TN also increases. Due to different ε Coulomb interaction is also different in the nanoparticles and in the surrounding region. It means that we can expect different Intrinsic and Extrinsic Coulomb blockades [8] in the process of device operations.

31.1.3 Intrinsic and Extrinsic Coulomb Blockades

In the present work, the simulation approach and the computer program described in [8, 9] is used. In memories with nanoparticles in the gate dielectric, retention characteristics are determined by the relationship between intrinsic and extrinsic Coulomb blockades (ICB and ECB) [9].

In the computer model the effective barrier U^* for ionization of electron No k from the TN is

$$U^* = U - \sum_{i=1}^{k-1} \frac{e^2}{\varepsilon r_{ik}}. \tag{31.3}$$

where r_{ik} is a distance between electrons No i and No k. As follows from expression (31.3) the effective barrier U^* decreases when the number of additional electrons in TN increases, and this dependence is caused by ICB.

The shallow traps surrounding TN accumulate electrons during the programming – erase operations and thus form a Coulomb barrier for an escape of trapped electrons from TN. This effect is known as ECB. Further we show that microscopic features of εinfluence significantly the relationship between ICB and ECB and, thus, the retention properties of memory device.

31.2 Influence of the Features of Dielectric Constant on Retention Properties of Memories

A computer simulation of retention properties of memory transistor has been performed using the approach developed by the authors of the papers [10, 11]. Retention quality is characterized by the life time of injected charge carriers inside TN. This value is proportional to the number of steps (N) in computer calculations. In computer experiments we used the input data corresponding to normal conditions of the device exploitation [11, 12].

In the input file the dielectric constant was expressed according to formulae (31.1) and (31.2). The results are shown in Figs. 31.1 and 31.2. In both cases the vertical axis shows the number of steps proportional to the life time of electrons in TN. The horizontal axis shows the values of dielectric constant for the bulk. It means that in simulation procedure dielectric constant was changed from $\varepsilon_V = 1$ ($x \approx a_0$) to the corresponding bulk value ε_V ($x \approx 10a_0$) indicated at the horizontal axis.

In Fig. 31.1, the upper curve (rhombs) corresponds to the case when in the simulation procedure the approach described by formula (31.1) is used.

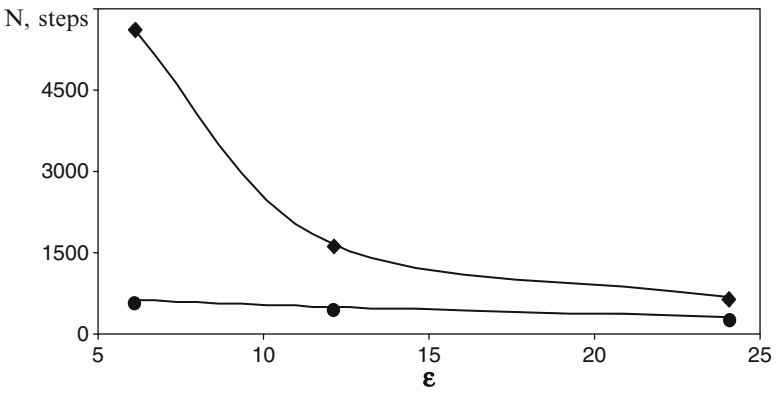

Fig. 31.1 Influence of the value of dielectric constant on the retention properties of memory device

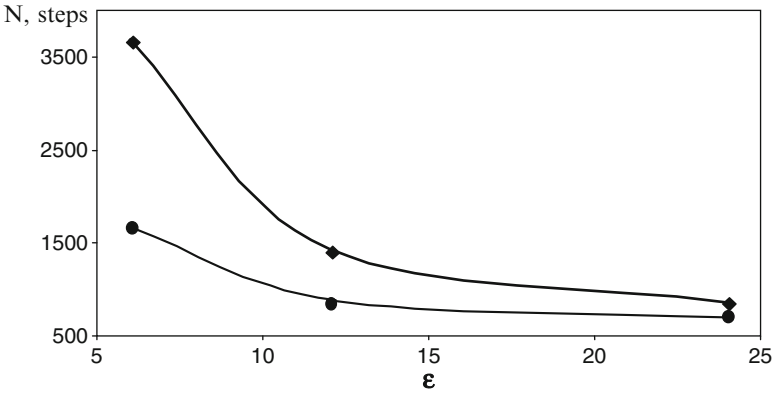

Fig. 31.2 Influence of the temperature on retention properties of memory device for two approaches for dielectric constants

The lower curve (circles) is obtained for the case when εdoes not depend on the distance. In the last case N does not depend on ε. It is explained by the same Coulomb repulsion in ICB and ECB. The upper curve shows that an approximation (31.1) allows revealing stronger Coulomb repulsion for ICB.

Figure 31.2 demonstrates the temperature dependence of retention properties of memory device for materials with different $\varepsilon$when approximation (31.1) is used. The upper curve (squares) is obtained for temperature 350 K and the lower curve (circles) for 600 K. We see that at accelerated temperatures the role of ε is weakened.

31.3 Conclusion

Computer modelling of retention characteristics of memory transistor with nanoparticles as charge traps in the gate dielectric has been performed. The influence of the microscopic behaviour of dielectric constant on the life time of trapped carriers in nanoparticles has been revealed. The interpretation of the results is given in terms of Coulomb blockades.

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